

REMARKS

Claims 1-21 and 23-33 are pending in the present application. Claim 22 is withdrawn. Claims 34-48 are cancelled. Claims 1-21 and 23-33 are rejected. New claims 49 and 50 are added above.

The Applicants note that the Office Action Summary does not indicate whether the drawings filed in the application are acceptable. Confirmation of their acceptability is respectfully requested.

The Applicants note that the Office Action Summary does not acknowledge the claim for foreign priority in the application and does not indicate whether a certified copy has been received. Acknowledgment is respectfully requested.

Claim 1 is objected to. Claim 1 is amended to recite "the bonding pads." Reconsideration of the objection to claim 1 is requested.

Claims 1-11, 16-17, 19, 21 and 23-30 are rejected under 35 U.S.C. 102(b) as being anticipated by Buynoski (U.S. Patent Number 6,246,118). Claims 12-15 and 31-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Buynoski and in view of Sundahl, *et al.* (U.S. Publication Number 2002/0084536). The applicant assumes that it was intended that claims 18 and 20 be included in the rejection under 35 U.S.C. 103(a). In view of the amendments to the claims and the following remarks, the rejections are respectfully traversed, and reconsideration of the rejections is requested.

In the present invention as claimed in claims 1-18, a semiconductor device includes a first portion and a second portion, and first and second groups of landing pads are formed in the first and second portions, respectively, of the semiconductor device. The landing pads are sized and shaped to be used with bonding pads. The first group of the landing pads is different than the second group of the landing pads. The semiconductor device further includes a plurality of the bonding pads formed over the first group of the landing pads and not formed over the second group of the landing pads, and a power supply line formed over the second group of the landing pads and not formed over the first group of the landing pads.

Claims 1-18 are amended to clarify that the plurality of bonding pads and the power supply line are formed over different groups of the landing pads. It is believed

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that these amendments to the claims clarify the distinctions between the claimed invention and the cited references.

In the present invention as claimed in claims 19-21 and 23-33, a semiconductor device includes a plurality of circuit blocks defining a center region between circuit blocks and an edge region at an edge of the circuit blocks. A first plurality of landing pads are formed in the center region and a second plurality of landing pads are formed in the edge region. A plurality of bonding pads are formed over one of the first plurality of landing pads and the second plurality of landing pads and not formed over the other of the first plurality of landing pads and the second plurality of landing pads and a power supply line is formed over the other of the first plurality of landing pads and the second plurality of landing pads and not formed over the one of the first plurality of landing pads and the second plurality of landing pads.

Buynoski discloses a device that includes six patterned metal layers Metal 1 - Metal 6 with five levels of conductive vias Via 1 – Via 5 electrically interconnecting features of spaced apart patterned metal layers. The Examiner asserts in the Office Action, at pages 2-3, section 4, that the Metal 1 is equivalent to the landing pads as claimed, that Via 1 is equivalent to the bonding pads as claimed, and that Metal 2 is equivalent to the power supply line as claimed. Every interconnection of Buynoski that includes Metal 1 also includes Via 1 and Metal 2, as Via 1 is connecting Metal 1 to Metal 2. Therefore, every portion of Metal 1 includes both the Via 1 and Metal 2.

Therefore Buynoski fails to teach or suggest a semiconductor device that includes a first group of landing pads being different than a second group of landing pads, a plurality of bonding pads formed over the first group of landing pads and not formed over the second group of the landing pads and a power supply line formed over the second group of landing pads and not formed over the first group of landing pads, as claimed in claims 1-18. Instead, in Buynoski, the Via 1 and Metal 2 are not formed on different portions of the landing pads independent of each other, but rather the Via 1 connects Metal 2 to Metal 1 and, therefore, Via 1 and Metal 2 are formed on the same portions of Metal 1. Buynoski further fails to teach or suggest a semiconductor device that includes a plurality of bonding pads formed over one of the first plurality of landing pads and the second plurality of landing pads and not formed over the other of the first plurality of landing pads and the second plurality of landing pads and a power supply line formed

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over the other of the first plurality of landing pads and the second plurality of landing pads and not formed over the one of the first plurality of landing pads and the second plurality of landing pads, as claimed in claims 19-21 and 23-33. Instead, in Buynoski, Via 1 and Metal 2 are both formed in all portions of Metal 1.

Buynoski fails to teach or suggest certain elements of the invention set forth in claims 1-18 and 19-21 and 23-33. Specifically, Buynoski fails to teach or suggest that suggest a semiconductor device that includes a first group of landing pads being different than a second group of landing pads, a plurality of bonding pads formed over the first group of landing pads and not formed over the second group of the landing pads and a power supply line formed over the second group of landing pads and not formed over the first group of landing pads, as claimed in claims 1-18, and a semiconductor device includes a plurality of bonding pads formed over one of the first plurality of landing pads and the second plurality of landing pads and not formed over the other of the first plurality of landing pads and the second plurality of landing pads and a power supply line formed over the other of the first plurality of landing pads and the second plurality of landing pads and not formed over the one of the first plurality of landing pads and the second plurality of landing pads, as claimed in claims 19-21 and 23-33. Therefore, it is believed that the claims are allowable over the cited reference, and reconsideration of the rejections of claims 1-11, 16-17, 19, 21 and 23-30 under 35 U.S.C. 102(b) as being anticipated by Buynoski is respectfully requested.

Sundahl, *et al.* discloses two interconnected circuit boards that include a front panel and a back panel which is electrically connected to the front panel via conductive connection points.

Sundahl, *et al.* fails to teach or suggest a semiconductor device that includes a first group of landing pads being different than a second group of landing pads, a plurality of bonding pads formed over the first group of landing pads and not formed over the second group of the landing pads and a power supply line formed over the second group of landing pads and not formed over the first group of landing pads, as claimed in claims 1-18. Sundahl, *et al.* further fails to teach or suggest a semiconductor device that includes a plurality of bonding pads formed over one of the first plurality of landing pads and the second plurality of landing pads and not formed over the other of the first plurality of landing pads and the second plurality of landing pads and a power supply line

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formed over the other of the first plurality of landing pads and the second plurality of landing pads and not formed over the one of the first plurality of landing pads and the second plurality of landing pads, as claimed in claims 19-21 and 23-33.

Hence, neither of Buynoski, as discussed above, and Sundahl, *et al.*, teaches or suggests certain elements of the present invention set forth in claims 1-18 and 19-21 and 23-33. Specifically, neither of the references teaches or suggests that a semiconductor device that includes a first group of landing pads being different than a second group of landing pads, a plurality of bonding pads formed over the first group of landing pads and not formed over the second group of the landing pads and a power supply line formed over the second group of landing pads and not formed over the first group of landing pads, as claimed in claims 1-18, and a semiconductor device includes a plurality of bonding pads formed over one of the first plurality of landing pads and the second plurality of landing pads and not formed over the other of the first plurality of landing pads and the second plurality of landing pads and a power supply line formed over the other of the first plurality of landing pads and the second plurality of landing pads and not formed over the one of the first plurality of landing pads and second plurality of landing pads, as claimed in claims 19-21 and 23-33. Accordingly, there is no combination of the references which would provide such teaching or suggestion. Neither of Buynoski and Sundahl, *et al.*, taken alone or in combination, teaches or suggests the invention set forth in the claims. Therefore, it is believed that the claims are allowable over the cited references, and reconsideration of the rejections of claims 12-15 and 31-33 under 35 U.S.C. 103(a) based on Buynoski and Sundahl, *et al.* is respectfully requested.

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In view of the amendments the claims and the foregoing remarks, it is believed that, upon entry of this Amendment, all claims pending in the application will be in condition for allowance. Therefore, it is requested that this Amendment be entered and that the case be allowed and passed to issue. If a telephone conference will expedite prosecution of the application, the Examiner is invited to telephone the undersigned.

Respectfully submitted,

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